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REMARKS/ARGUMENTS

Applicants gratefully acknowledge the indication that claims 10-11, 14-17, 19, 31, 35-36 and 38 are allowed. In light of the above amendments and the remarks below, it is respectfully submitted that all pending claim are allowable.

Pending claims 1 and 3-5 stand rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,579,261 (Radjy). Applicants respectfully traverse the rejection and respectfully request reconsideration of the same, as claim 1 has been amended to include the subject matter of dependent claim 7. As the Office Action concedes that Radjy nowhere teaches providing a control negative voltage to a substrate of a transistor of a decoder that is coupled to pass a negative voltage to at least one deselected wordline, claim 1 and claims 3-5 are patentable over Radjy.

Pending claims 1, 3-4, 9, 22-25, 27-30, and 32-33 stand rejected under 35 U.S.C. §102(e) over U.S. Patent No. 5,537,362 (Gill). Applicants respectfully traverse the rejection and respectfully request reconsideration of the same. As to claim 1, the Office Action contends that Gill teaches supplying a negative voltage to at least one deselected wordline during a programming operation on a selected wordline. Applicants respectfully disagree. In this regard, the Office Action refers solely to the abstract of Gill for such a teaching. However, all that Gill teaches is that *during a read operation*, a negative voltage is provided to deselected wordlines. However, Gill never teaches or suggests supplying such a negative voltage during a programming operation. In fact, Gill plainly teaches the opposite. That is, as shown in Table 1 of Gill, during a programming (i.e., write) operation, a ground voltage is supplied to deselected wordlines, not a negative voltage. Instead, as shown in Table 1, the only time a negative voltage is provided to deselected wordlines is during a read operation. For at least this reason, claim 1 and the claims depending therefrom are patentable over Gill.

With respect to claim 22, Gill nowhere teaches a decoder that includes a first transistor of a first polarity to pass a negative voltage to a deselected wordline and a second transistor of a second polarity coupled to the first transistor to pass a program voltage. In this regard, the Office Action refers to FIG. 5 of Gill, and more specifically to multiple pMOSFETs 62. However, both of these MOSFETs are of a single polarity. Furthermore, these MOSFETs are not even of a decoder. Instead, these transistors of Gill are part of a voltage regulator that receives a signal from a decoder. Gill, col. 8, lns. 5-21. However, they are not part of the

decoder itself. Furthermore, these transistors of Gill do not pass a negative voltage if the wordline is deselected for programming and instead a program voltage if the wordline is selected for programming. Accordingly, claim 22 and the claims depending therefrom are patentable.

The rejection of claim 22 is further traversed, as there is no basis for contending that the recited wireless interface coupled to a non-volatile memory is somehow inherent in the system of Gill. "In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily flows* from the teachings of the applied prior art." *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis added). That is, to meet the inherency requirement, Gill must *necessarily* require a wireless interface coupled to a non-volatile memory. As the Office Action concedes that such an interface is "optional," inherency cannot be established and the rejection is overcome. Accordingly, claim 22 and the claims depending therefrom are patentable over Gill.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

Date: \_\_\_\_\_

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Mark J. Rozman  
Registration No. 42,117  
TROP, PRUNER & HU, P.C.  
1616 S. Voss Road, Suite 750  
Houston, Texas 77057-2631  
(512) 418-9944 [Phone]  
(713) 468-8883 [Fax]  
Customer No.: 21906